Future TCAD system for nanometer-scale-device manufacturing using plasma etching

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Abstract. The present stage of a series of numerical modelings of the plasma etching processes is overviewed. Physical, chemical and electrical linkage among modules describing low temperature plasma structure/function in a reactor, the profile and local charging evolution in a hole/trench, and electrical device damage during etching will make it possible to prepare a technology computer aided design (TCAD) for the practical purpose of prediction and designing the etching process. This system will also help to determine device arrangement and size in system on a chip (SoC) in a closed integration system. TCAD will also provide a tool for discussing the etching processes between process engineers and device designers in the age of nanometer-scale device technology.

I INTRODUCTION

Low pressure radio-frequency (rf) glow discharges, named *low temperature plasmas*, have been widely used in microelectronic device fabrication and new material manufacture. They differ from dc glow discharge plasmas in that the plasma is maintained even in an electrodeless chamber as well as between metallic and/or dielectric electrodes. They are used to produce chemically activated neutrals (radicals) and ions responsible for surface reactions in plasma etching and in plasma chemical vapor deposition.

The 1999 edition of the International Technology Roadmap for Semiconductors (ITRS) targeted the current needs in nanometer-scale-device manufacturing [1]. Circuit integration will progress from the present system on a chip (SoC) (or ultra large scale integrated circuit; ULSI) with 10^7 transistors to that with 10^9 transistors with a 70 nm gate length, operating with a 10 GHz clock frequency at a 1 % activity level in 2008 [1]. It is considered that the functional throughput of SoC in 2008 may be compared with that of the human brain, which has 10^{15} synapses operating effectively with a 1 kHz clock frequency at a 0.1 % activity level [2]. The achievement of the SoC's high speed operation arises from two directions. One is the further shrinkage of device dimension. The other is the use of a multi-interconnect from 6 to 9 layers to reduce the signal delay in the interconnect. Therefore, future progress in SoC development depends strongly on manufacturing technology to produce nanometer-scale devices by means of plasma etching, while miniaturization requires optimization of each of the processes involved in the technology.

Currently there is no general rule for designing the plasma etching. Under these circumstances, the industry research laboratories have focused on the challenges posed by plasma chemical issues in the development of next-generation plasma processing and the tools [3]. We, however, believe that further optimization of the plasma structure should be achieved first and plasma chemical kinetics should be optimized later as the changes in the former may strongly affect the latter. Modeling of the plasma structure and its function in the etching reactor has been in development during the past 15 years [4]. Microscopic profile evolution of a patterned wafer and microloading during etching have been simulated independently of macroscopic plasma modeling in reactors. Plasma damage to the device during etching has been experimentally studied.

In line with the roadmap, continuous improvement of tools and processing methods will extend to the reduction of the size of the features of a chip. In parallel with the development of this hardware, the coming

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14. ABSTRACT
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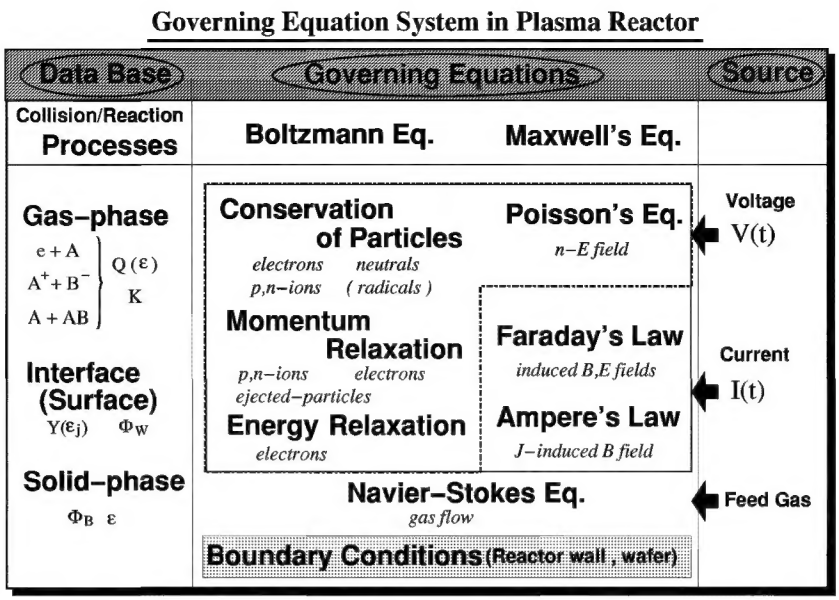

FIGURE 1. Governing equation system in a low temperature plasma prediction in an etcher and related quantities.

decade will bring fabrication methodology in the field of process integration. One of the promising procedures for this purpose will be the prediction of the plasma structure and processing on the wafer with the aid of numerical modeling over the entire reactor system. This will be achieved by means of the data base regarding the fundamental collision and reaction processes both in a gas phase and on the wafer surface. That is, practical application of *technology computer aided design* (TCAD) will extend into the backend processes, especially in plasma etching, in addition to the frontend processes, in order to elaborate the optimum conditions between the device designer and the process engineer.

In this paper, we propose a series of modelings of a low temperature plasma structure and the function in a reactor, of profile evolution and charging in a patterned wafer, and of device damage during plasma etching by using modules for each of objectives. Prediction of plasma damages to a nanometer-scale-device structure during etching will be discussed in a two-frequency capacitively coupled plasma (2f-CCP) reactor by using the series of modeling.

II OVERVIEW OF PROPOSED TCAD SYSTEM

The system proposed here for the purpose of backend process prediction, in particular, for plasma etching involves a gas phase module, surface phase module, and bulk device module. The gas phase module provides macroscopic plasma structure/function, and the feed gas flow and particle flow produced in the gas phase and on the wafer in the plasma etcher in a self-consistent manner by using an extended relaxation continuum (E-RCT) model under the data base of microscopic collision processes and external plasma conditions. It uses, at need, direct numerical procedure (DNP) of the phase space Boltzmann equation under the result of the plasma structure to predict the velocity or energy distribution of ions and electrons. The surface module works as a temporal profile predictor at etching and for predicting plasma damage. The bulk device module predicts the critical size of the device element in SoC (or ULSI) by the aid of plasma parameters under the circumstances of trench/hole size and a geometrical antenna profile.

It aims at an optimum plasma design in a reactor and at the avoidance of plasma damage during etching by means of low temperature plasma control or revision of the device arrangement and the size. The system will provide a tool to align the backend etching process between the process engineer and the device designer.

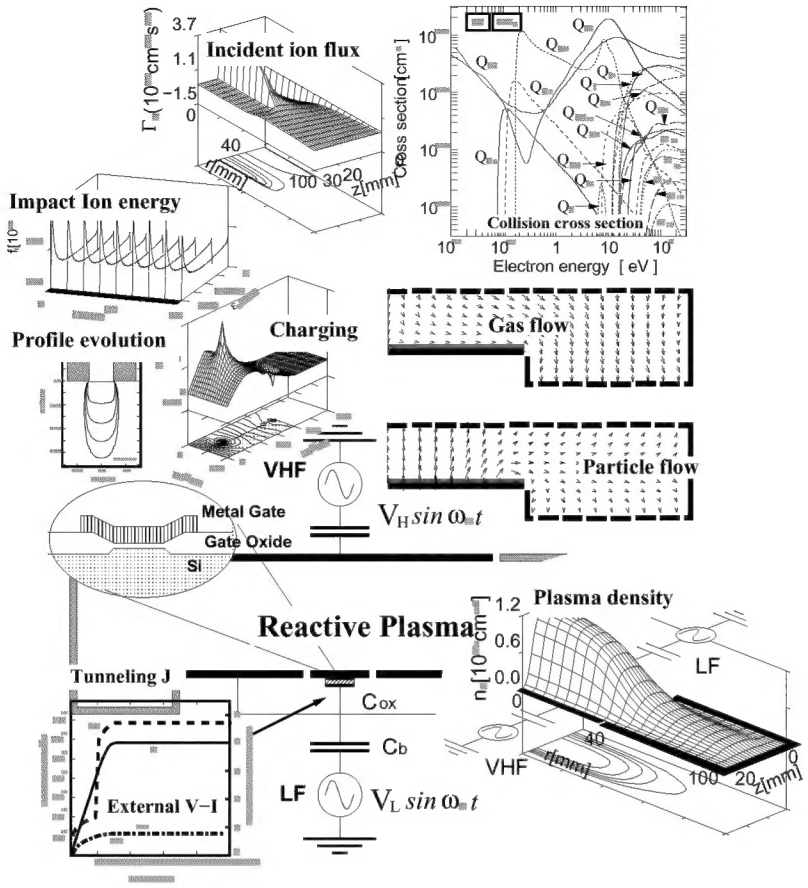

FIGURE 2. Overview of a series of modelings of plasma structures in a two-frequency capacitively coupled reactor, plasma etching, and related damage prediction.

III PLASMA ETCHING REACTOR

The low-temperature plasma used in micro- and nano-electronic device manufacturing is maintained even in an electrodeless chamber as well as between metallic and/or dielectric electrodes. A compact apparatus with high and uniform plasma density is required for the next generation of the etching reactor, which will have a high rate of surface treatment on a large-area wafer. High density plasma is produced by using an ac power source in the range of high-, very high-, and ultra high-frequencies with or without the aid of external magnetic field. The dry etching reactor is classified into three types according to the coupling system between the external ac power source and the plasma. These are named *capacitively coupled-, inductively coupled-, and antenna coupled-plasmas.* The wafer to be processed in the reactor is usually biased by a low frequency voltage source in order to obtain anisotropic etching with high efficiency.

Plasma etching is applied to metal(Al), Poly-Si, and dielectric(SiO_2, low-k materials). Metal and Poly-Si etching use a high density plasma with low energy ions on the wafer, while the latter oxide etching is executed by ion-assisted processing using a few hundred eV or more.

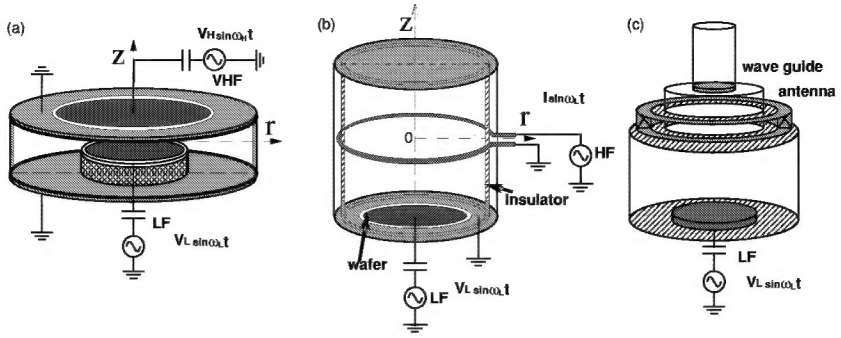

FIGURE 3. Schematic diagram of plasma etchers classified in terms of the coupling between ac power source and plasma. (a)capacitively coupled plasma (CCP), (b)inductively coupled plasma (ICP), and (c)antenna coupled plasma (ACP) reactors.

A Two-frequency capacitively coupled plasma structure and its function

The modern oxide etcher has to separate the function of plasma sustaining and biasing electrodes. In our previous paper, separation of the effects of rf sources used for biasing the wafer and for sustaining the plasma was experimentally studied using a computerized tomography (CT) image of the spatiotemporal net emission rate for a *two-frequency capacitively coupled plasma* (2f-CCP) [5]. It was shown that almost complete *functional separation* is achieved in the 2f-CCP system in that the plasma is produced and sustained at the electrode operating at very high frequency (VHF), 100 MHz, and the high energy ion for etching is generated at low frequency (LF) bias electrode without interaction between both of power sources. Pulsed operation of the plasma source under CW biasing was also investigated and much higher system performance was achieved. As a result, 2f-CCP operated by a VHF-LF system will achieve the following two goals: 1)Full separation of the effects of sustaining and biasing powers allows precise adjustment of the properties of ions hitting the wafer surface without perturbing the plasma. 2)The reduction of excessive dissociation improves the selectivity of the etching in the CxFy/Ar system.

With reducing the device's dimension, the high aspect ratio etching of the contact hole or trench is influenced by a local charge accumulation inside the structure. This is known as anomalous etching. Otherwise, charging on metal in a period of over-etching causes critical damage to the thin gate oxide, known as *antenna effect* [6]. The damages to the wafer with topographically different surface structure are intrinsic to high density plasma etching. Figure 5 describes the predicted axial number density distributions of the charged particles and the metastable argon in temporally averaged form, obtained by the RCT modeling. The plasma density with 10^{11}cm^{-3} spreads widely between both electrodes due to the influence of the spatial trapping of low energy electrons, as compared with that driven by the HF(13.56 MHz)-LF system. In order to overcome plasma damage occurring during the etching process, pulsed operation of a high density plasma source was proposed in order to aim at the control of positive and negative charge flux to the surface during the on/off period [7]

B Ion velocity distribution incident on wafer

Oxide etching requires a high energy ions incident on the patterned wafer. The energy is distributed between 200 eV to 1000 eV in order to obtain a sufficient etching yield of oxide under the ion assisted mode in feed gases based on Ar and fluorocarbon mixture.

One of the physical issues in oxide etching is the prediction of the velocity distribution of ions incident on the wafer as a function of frequency and amplitude of the bias voltage, though a number of experimental distributions have been observed. As is well-known, at high frequency that the ion does not have sufficient time to cross the space between the electrodes during the half-period, the ion transport is characterized in a time averaged-fashion. Thus, the ion velocity distribution is estimated as a function of distance from the

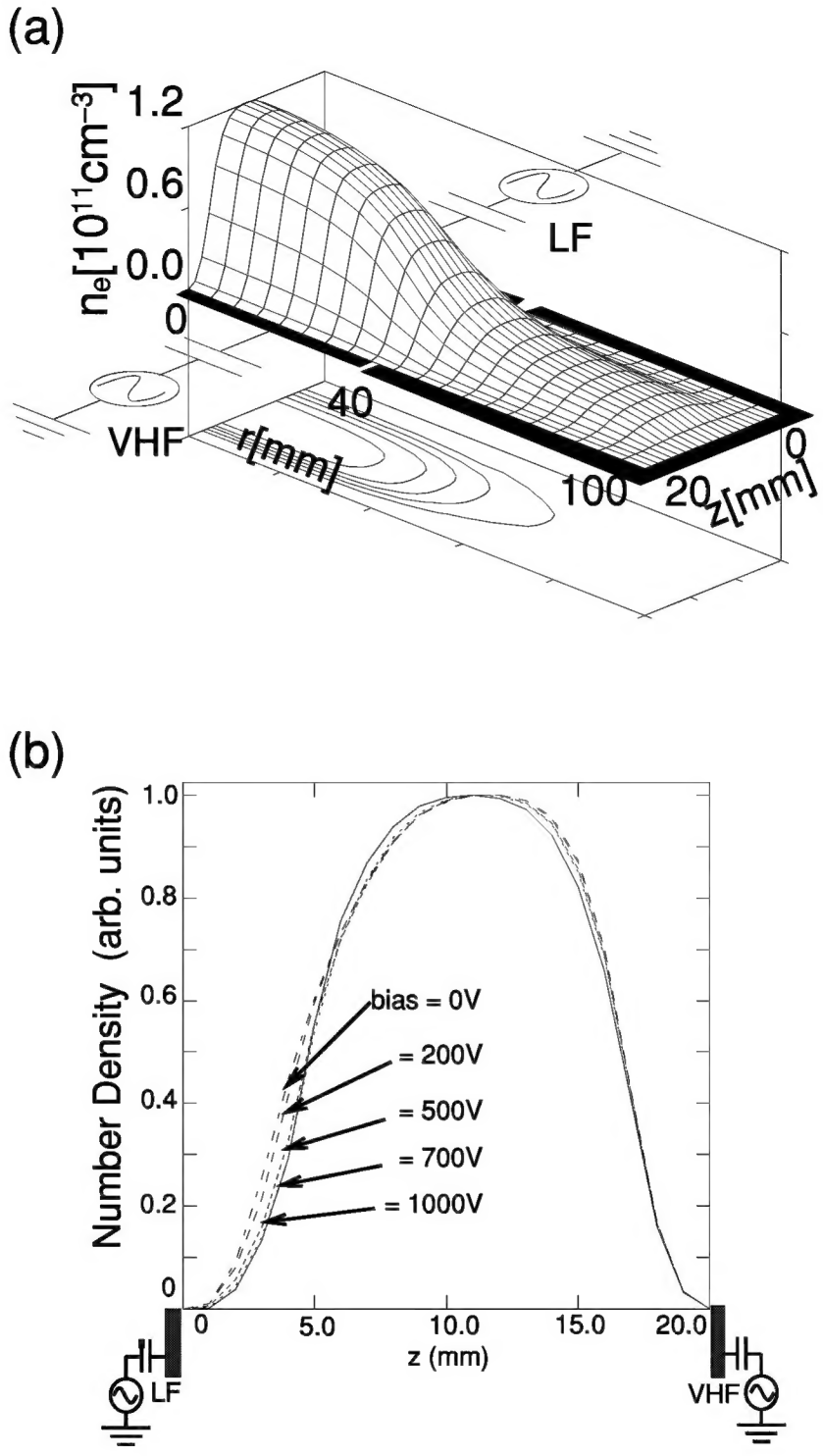

FIGURE 4. Example of the functional separation in oxide etcher in 2 frequency-CCP reactor, sustained for 25 mTorr, 10 sccm in CF_4/Ar at (a)13.56 MHz, 300sin ωt-270 V, and (b)100 MHz, 50sin ωt-16 V. The bias voltage is shown (ref. Kitajima1, et.al.)

sheath-bulk plasma boundary. This means that a time-independent Boltzmann equation can predict with validity the distribution at high and very high frequency ranges [8]. We show the typical example of the energy

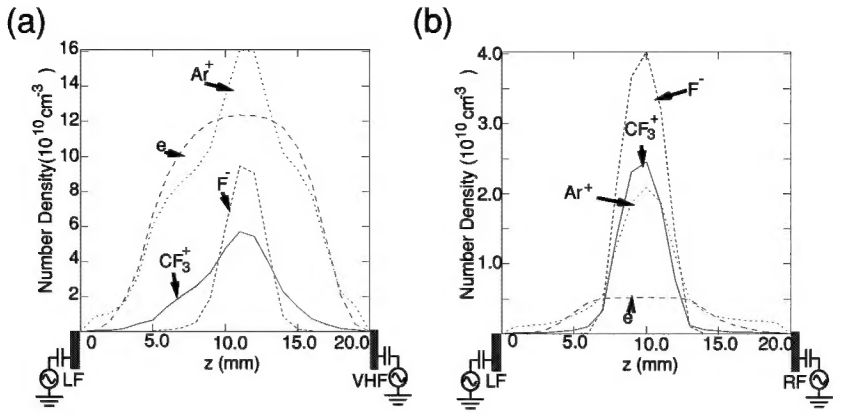

FIGURE 5. Predicted axial number density distributions of species in 2f-CCP, excited at 100 MHz, 300 V, and biased at 678 kHz, 200 V at 50 mTorr in CF_4/Ar.

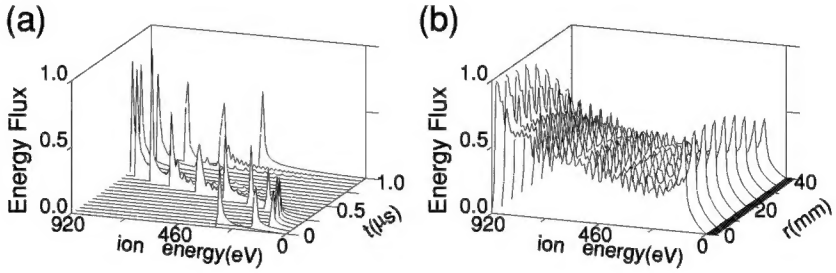

FIGURE 6. Ion energy distribution on the electrode as a function of radial distance in 1f-CCP driven at 100 MHz and 300 V at 50 mTorr in $CF_4(5\%)$/Ar.

distribution of ions incident on the electrode driven at 100 MHz and 300 V at 50 mTorr in $CF_4(5\%)$/Ar in 1f-CCP.

Since at low frequencies an ion will temporally relax the energy to the instantaneous field, we have to consider the space and time characteristics of the ion velocity by using the time-dependent Boltzmann equation. It is difficult, in general, to numerically analyze the spatiotemporal migration of a beam-like quantity due to the presence of numerical diffusion in the differential equation. Even in the prediction of a spatiotemporal ion transport to the wafer, supplied from the sheath-bulk plasma boundary, the circumstances are the same as those of a beam-like ion transport, and therefore it is still under consideration.

C Ejected nonvolatile particle transport

The nonvolatile particle, ejected nonuniformly from the wafer surface by the impact of energetic ions during etching, is transported from the surface through a high sheath field region with initial nonthermal energy under the circumstances of the external feed gas flow in the reactor. A finite amount of the etched particles will be reabsorbed on the wafer surface by back diffusion, ionized mainly between the sheath and the bulk plasma, or deposited on the reactor wall. The nonvolatile particles may accumulate and coagulate with each other at specific points or regions in the reactor. Otherwise, they will be pumped out with a feed gas. In our previous paper, we numerically described the transport proper to the nonvolatile particles in a conventional parallel plate reactive ion etcher (RIE) excited at 13.56 MHz and 100 MHz respectively, i.e., 1f-CCP [9]

Figure 7 shows the 2D density distribution of the Si atom steadily ejected from the wafer of 140 mm in diameter in 1f-CCP driven at 100 MHz and an amplitude of 300V at 50 mTorr in $CF_4(5\%)$/Ar. The spatial

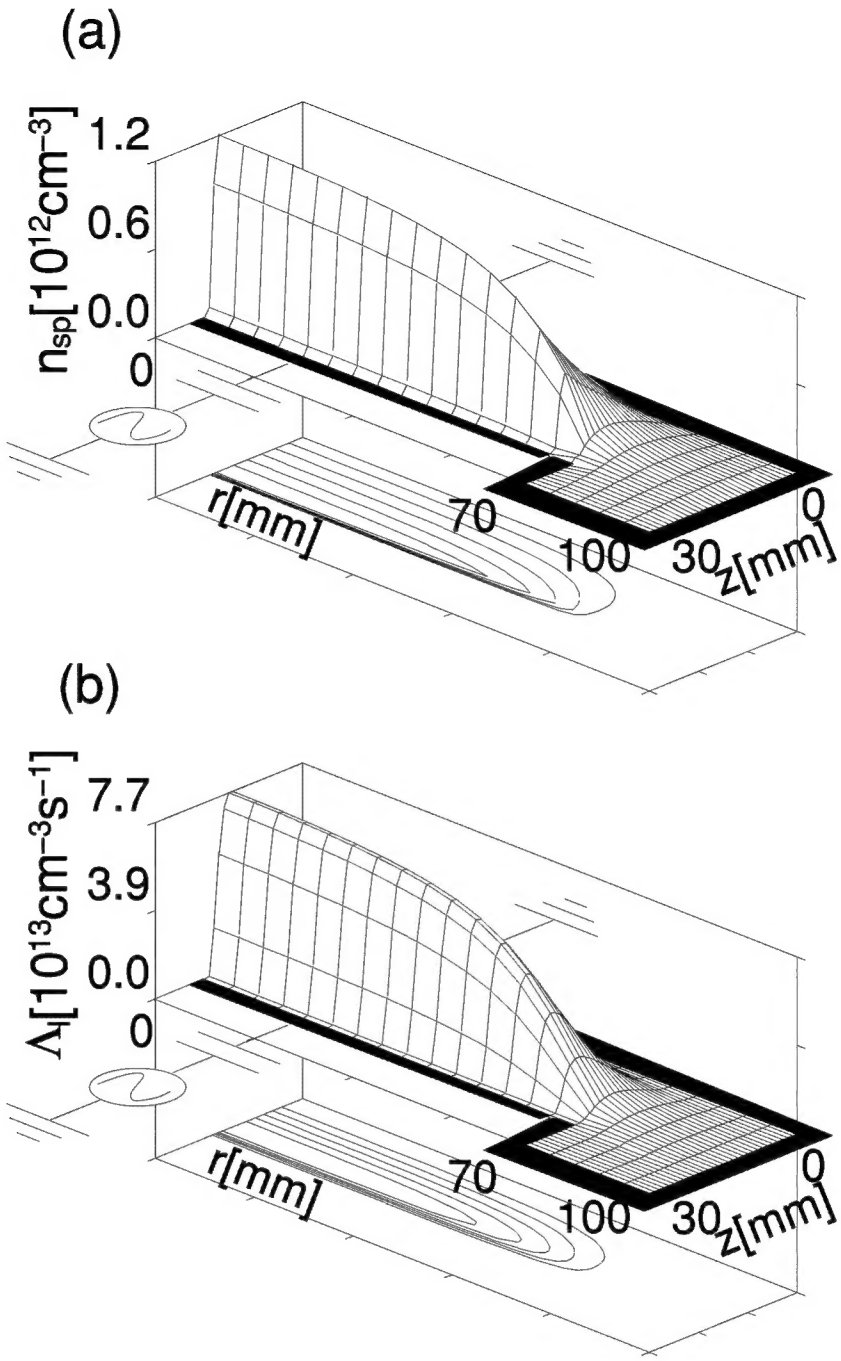

FIGURE 7. Ejected Si atom from the wafer. (a)2D density distribution of neutral Si. (b)2D net ionization rate of Si. External conditions are the same as those in Fig.6.

distribution with the axial peak at 3 mm from the wafer is the result of the collisional energy relaxation of the ejected neutral Si atom with the feed gases, and of the ionization by the electron impact, since the ionization threshold, 8.15 eV is much lower than that of the feed gases, Ar and CF_4, 15.6 eV and 16 eV. In fact, the effect of the ionization reduces the neutral Si density by 6 %. It is reported that in a high density plasma with $10^{12}cm^{-3}$ at low pressure, almost 50 % of the ionization to sustain the plasma is supplied by way of the ejected metallic atom. These will change the original plasma structure maintained purely in the feed gas.

The exhaustive path of nonvolatile particles ejected with an initial nonthrmal energy at the wafer surface is

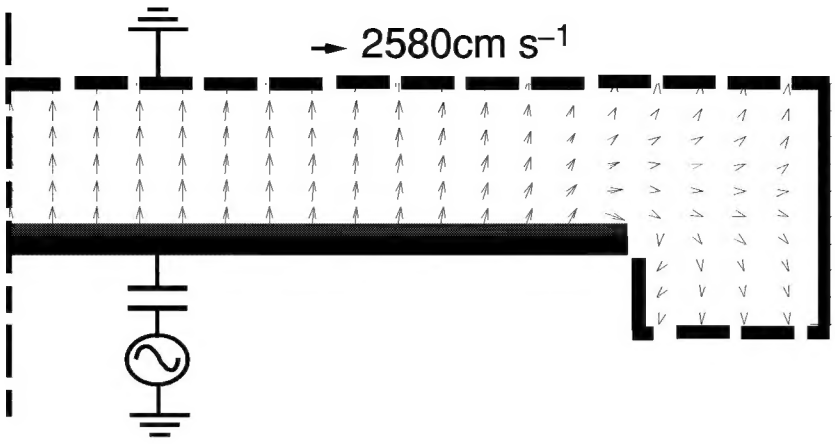

FIGURE 8. 2D flow velocity distribution of the ejected Si atom. External conditions are the same as those shown in Fig. 6.

practically important for the reactor design, as well as the feed gas flow. Flow design of the feed gas, supplied from the showerhead on the electrode, is a well-established technique obtained by the Navier-Stokes equation or Direct Simulation Monte Carlo (DSMC) [10,11]. In particular, DSMC is suited for the problem of rarefied gas dynamics. At intermediate pressure, 25 mTorr - 50 mTorr, the momentum transfer theory can effectively estimate the transport of the nonvolatile particles as shown in the form of 2D flow velocity distribution in Fig. 8(See ref [9]). It can be concluded from this typical example that the flow pattern of the nonvolatile particle is completely different from the feed gas flow in the oxide etcher.

IV CHARGING INSIDE A MICRO STRUCTURE

By increasing the device integration and shrinking the SoC's, or ULSI's size, topographical nonuniformity and/or potential localization on the microscopically patterned-wafer will be provided during plasma etching for a high aspect ratio or large antenna ratio hole/trench. Under these circumstances, technological development in uniform etching without producing microloading (RIE-lag) and damage is an urgent issue in plasma processing.

A Microtrench and etch stop

We have numerically investigated the influence of physical and electrical properties of plasma etching on the inside of a micro trench in SiO_2 by studying the growth of the local potential by using Monte Carlo simulation of ion and electron transport [12]. When the aspect ratio increases, the bottom is charged to the potential sufficient to prevent all the incident ions within the period of monolayer stripping under a practical set of conditions, and the etch stop occurs. Figure 9 shows the temporally saturated potentials on the top part of the side wall and the trench bottom as a function of aspect ratio [12]. In a practical RIE with a typical fluxes of $10^{16}\text{cm}^{-2}\text{s}^{-1}$ of electrons and ions, and an etch rate of 500 nm min^{-1}, a monolayer in SiO_2 is apparently stripped at intervals of hundreds of ms.

Under these circumstances, we will predict the relations of the time constant between the charging (τ_{charge}) and the monolayer stripping (τ_{MLetch}) at very high aspect ratio etching, $\tau_{charge} \leq \tau_{MLetch}$. The results show that charging may become the cause of etch stop and associated problems in oxide etching at high aspect ratios. It is still possible that both chemical and physical mechanisms may occur at the same time, because the mechanism presently described is the limiting mechanism as it is dependent only on geometry and on the initial conditions. More complex plasma chemistry may lead to a different type of ion that provide different

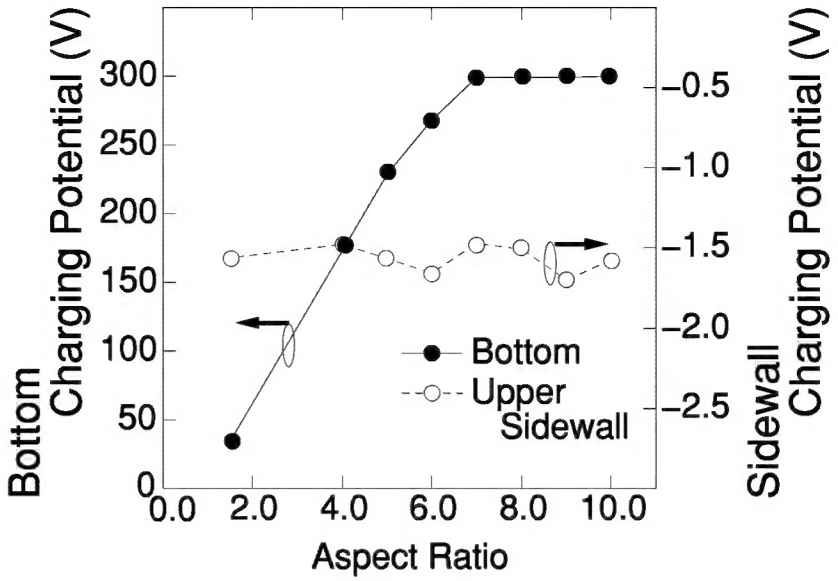

FIGURE 9. Charging potential's dependence on aspect ratio at the bottom and the top of the sidewall of SiO_2 trench in the system struck by beam-ions with 300 eV and thermal electrons of 3 eV. (ref.Matsui, et.al.).

plasma potentials, or may allow conductive deposition at the side wall or a conductive thin layer at the bottom [3].

B Gate oxide damage

Oxide breakdown of gates of the transistors in SoC was found in the system that being over-etching of the contact hole in SiO_2 and in the metal etching system (See Fig.10). The presence of a locally strong imbalance of the surface charge on the bottom with respect to a base potential in Si-wafer is the origin of the thin gate oxide damage during plasma etching. Marked gate damage is observed in an etching in a high density plasma reactor. In a multi-interconnect with 6-10 layers, via hole over-etching will be a new candidate for the source of gate oxide damage. Gate oxide damage is intrinsic to the pattern with a high aspect ratio and/or a large antenna ratio during plasma etching.

Figure 10(a) shows a simple model device structure, exposed to the biased-low temperature plasma, in order to investigate the temporal characteristics of the charge accumulation inside the trench and to estimate the damage to the gate oxide during plasma etching as a function of aspect ratio and antenna ratio. Device arrangement and size will constitute the design and process parameters to be estimated. A typical example of predicted gate damage is shown in Fig.10(b).

V CONCLUSIONS

Anomalous etching (micro loading) in metal, Poly-Si, and SiO_2, and gate oxide damage during plasma etching are experimentally observed through processes of the further integration and the shrinkage of the device. These are urgent issues in SoC manufacturing. These phenomena are caused by the local charging of positive ions and electrons inside micro- and nano- structures, and are considered as functions of aspect ratio and antenna ratio on patterned wafers exposed to plasma.

Locally distributed surface charging will be one of the interesting phenomena in future nano-technologies using low temperature plasma, because the physical mechanism of the local charging inside the micro/nano structure exposed to the plasma is based on two proper and general characteristics of plasma, i.e., the quasi-neutrality of charges and the incident flux equality under different range of energies on a surface.

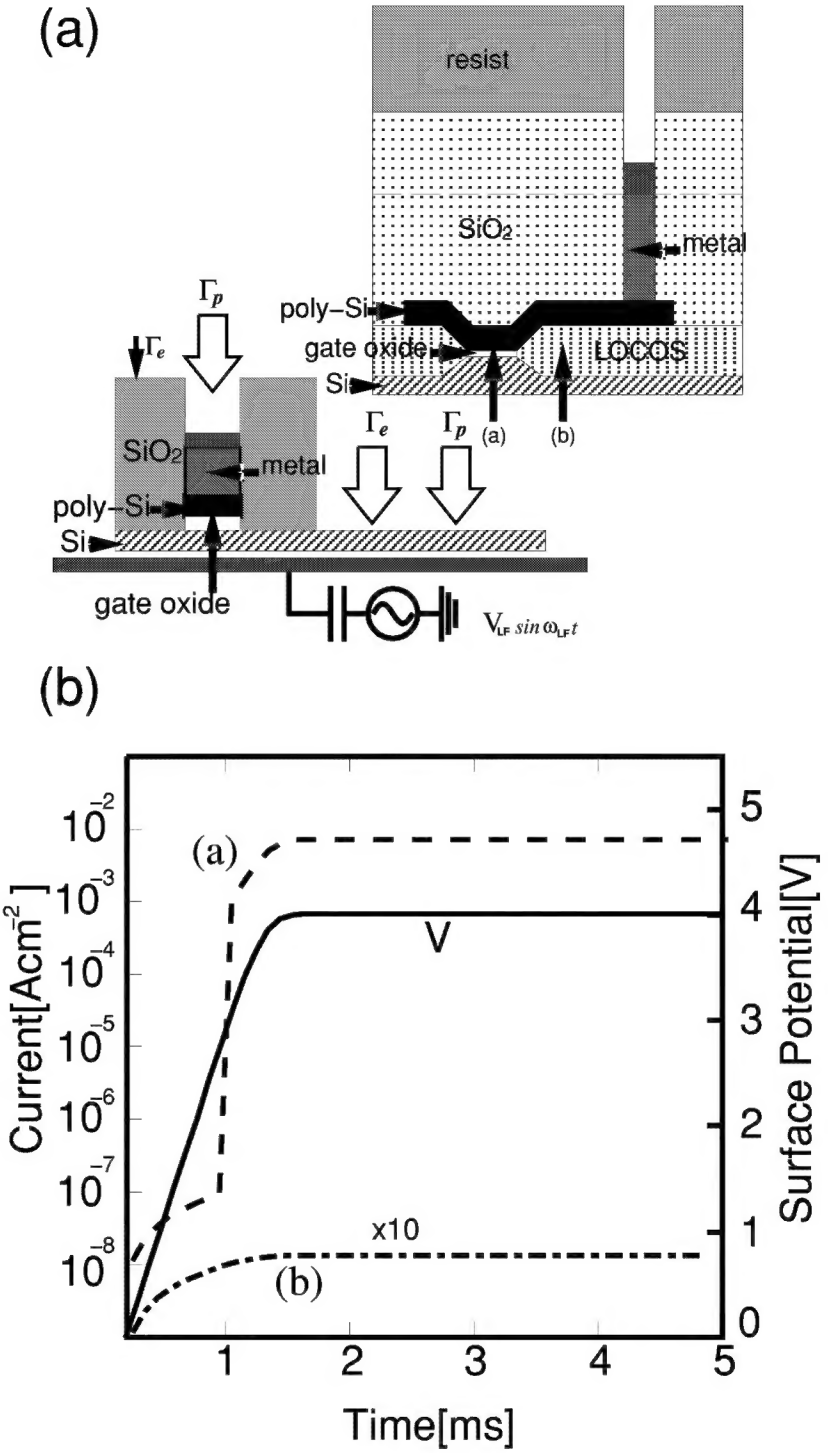

FIGURE 10. Simple model of the device structure for the study of gate oxide damage as a function of aspect ratio and antenna ratio(a), and an example of the predicted temporal gate damage caused by direct tunneling current during plasma etching.

Numerical modeling of a low temperature plasma in a reactor, profile evolution, local charging in a hole or trench, and electrical device damage during plasma etching have been for the most part investigated independently of each other for the last 15 years in the USA, Japan and Europe. Physical, chemical, and electrical

linkage among these modules will make it possible to prepare a TCAD for the practical purposes of the prediction and design of the etching process, and of device arrangement and the size in SoC in a closed integration system. In addition, the present proposed TCAD will provide a tool for the discussion of the etching processes between process engineers and device designers.

It will be finally stated that the practical success of the prediction and design of the etching process by using TCAD will depend largely on the presence of the data base regarding gas and surface phases. It must be strongly emphasized in order to avoid a data base crisis in TCAD application that it is increasingly essential to study fundamental collision/reaction processes both in atomic/molecular and in surface physics and chemistry.

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